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10/598,151	06/07/2007	Syuichi Kikuchi	24179965-000006	1657

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BAKER & MCKENZIE LLP
PATENT DEPARTMENT
2001 ROSS AVENUE
SUITE 2300
DALLAS, TX 75201

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,151	KIKUCHI, SYUICHI	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/18/06, 6/6/07, 3/19/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed June 07, 2007, the Information Disclosure Statement filed August 18, 2006, the Information Disclosure Statement filed June 6, 2007, Information Disclosure Statement filed March 19, 2008, and the Foreign Priority filed August 18, 2006.

2. Claims 1-13 are pending. Claims 1, 9, 10, 11, 12, and 13 are independent.

Information Disclosure Statement

3. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on August 18, 2006, June 6, 2007, and March 19, 2008. These IDS has been considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. The abstract of the disclosure is objected to because the following minor informalities: legalese.

In the Abstract, line 1, it is suggested to change "Disclosed is a programmable" to --Discussed is a programmable--.

Correction is required. See MPEP § 608.01(b).

6. The disclosure is objected to because of the following informalities:

In the Specification, page 5, last few words of line 24, it is suggested to change "the signal ***form*** the node of the" to --the signal **from** the node of the--.

Appropriate correction is required.

Claim Objections

7. **Claims 10 and 11 are objected to** because of the following informalities: minor cosmetic adjustments (it is suggested to change "**at at**" to --**in at**-- so as to promote clarity during publication). The intended meaning of the phraseology indicated (see below for exact page and line numbers) appears to be understood, but it appears that the pre-grant publication (see U.S. Patent Application Publication 2007/0296457) omitted one "at" of the "**at at**" phraseology for claim 10 and claim 11. A suggestion for correction to claims 10 and 11 is presented to aid and promote clarity at time of publication for the instant application's Patent (should it mature into a Patent).

In Claim 10 (page 33, line 11), it is suggested to change "**at at** least one of a plurality of ordered" to --**in at** least one of a plurality of ordered--.

In Claim 11 (page 34, line 11), it is suggested to change "**at at** least one of said memory positions" to --**in at** least one of said memory positions--.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. **Claims 13 and 14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** Claims 13 and 14 are both drawn to a "program" which does not appear to fall within any of the following statutory categories: process, machine, manufacture, or composition of matter, or any improvement thereof.

Allowable Subject Matter

10. **Claims 1-12 are allowed.**

11. The following is a statement of reasons for the indication of allowable subject matter:

With respect to independent claim 1, there is no teaching, suggestion, or motivation for combination in the prior art to a programmable logic circuit control system including a controller which controls the logical structure of the programmable logic circuit, a module memory which stores a plurality of modules each module having data defining the logical structure, a module designation memory which stores data

designating an address of a module in at least one a plurality of ordered memory areas and further storing a read address and a write address associated with a module, a node value memory with memory areas for writing a value represented by a signal generated at a predetermined node of the programmable logic circuit in that memory area to which a write address is allocated and for supplying the programmable logic circuit with a signal representing a value stored in that memory area to which a read address is allocated, the controller additionally has a function of acquiring data stored in a memory area of the module designation memory, a function of acquiring a module indicated by an address included in the data acquired from the module designation memory and generating a control signal for causing the programmable logic circuit to take a logical structure indicated by the module and supplying the control signal to the programmable logic circuit to change the logical structure of the programmable logic circuit, and a function of supplying a read address and a write address included in the data acquired from the module designation memory to the node value memory.

With respect to independent claim 9, there is no teaching, suggestion, or motivation for combination in the prior art to a programmable logic circuit control apparatus having an acquiring section to acquire data stored at a memory position in a module designation memory, which stores data designating an address of a module in at least one of a plurality of ordered memory positions, wherein a read address and a write address allocated to a memory position in a node value memory are further stored at that memory position in the memory positions in the module designation memory where data designating the address of the module is stored, wherein the node value

memory stores a value represented by a signal generated at a predetermined node of the programmable logic circuit, at a memory position to which a write address is allocated, and supplies a signal representing a value stored at a memory position to which a read address is allocated, to the programmable logic circuit, wherein the programmable logic circuit control apparatus additionally has a write-address supply section to supply a write address included in the acquired data to the node value memory, a change section to acquire a module indicated by an address included in the acquired data from a module memory and to take the logical structure from the module to change the logical structure of the programmable logic circuit, and a read-address supply section to supply a read address included in the acquired data to the node value memory.

With respect to independent claim 10, there is no teaching, suggestion, or motivation for combination in the prior art to a programmable logic circuit control method which acquires a module being of data defining a logical structure of a programmable logic circuit to be controlled, and changes the logical structure of the programmable logic circuit to be controlled based on the acquired module having the steps of storing a plurality of modules each module includes data defining the logical structure, acquiring data designating an address of a module and a signal generated at a predetermined node of the programmable logic circuit, and stores a read address and a write address, allocated to that memory area in the node value memory which stores a value represented by the signal, in (see claim objection) at least one of a plurality of ordered memory positions for module use order designation, acquiring data stored at the

memory positions for module use order designation, supplying a write address included in the acquired data to the node value memory, acquiring a module indicated by an address included in the acquired data from the module memory, generating a control signal to cause the programmable logic circuit to take a logical structure indicated by the module, and supplying the control signal to said programmable logic circuit to change the logical structure of the programmable logic circuit, and supplying a read address included in the acquired data to the node value memory, wherein the node value memory has a function of storing a value represented by a signal generated at a predetermined node of the programmable logic circuit, at a memory position to which a write address is allocated, and a function of supplying a signal representing a value stored at a memory position to which a read address is allocated, to the programmable logic circuit.

With respect to independent claim 11, there is no teaching, suggestion, or motivation for combination in the prior art to a programmable logic circuit control method which acquires a module being of data defining a logical structure of a programmable logic circuit to be controlled having a function of changing the logical structure according to a supplied control signal, from a module memory storing a plurality of modules, and generates a control signal for causing the programmable logic circuit to be controlled to take a logical structure indicated by the acquired module and supplies the control signal to said programmable logic circuit to be controlled, thereby changing the logical structure of the programmable logic circuit to be controlled, having the steps of acquiring data stored at a memory position in a module designation memory, which has

a plurality of ordered memory positions and stores data designating an address of a module in (see claim objection) at least one of the memory positions, from the module designation memory, wherein a read address and a write address allocated to a memory position in a node value memory are further stored at that memory position in the memory positions in the module designation memory where data designating the address of the module is stored, and the node value memory has a function of storing a value represented by a signal generated at a predetermined node of said programmable logic circuit to be controlled, at a memory position to which a write address locally supplied is allocated, and a function of supplying a signal representing a value stored at a memory position to which a read address is allocated, to the programmable logic circuit, supplying a write address included in the acquired data to the node value memory, acquiring a module indicated by an address included in the acquired data from a module memory, and changing a logical structure of the programmable logic circuit to a logical structure indicated by the module, and supplying a read address included in the acquired data to the node value memory.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Popli et al. (U.S. Patent 5,336,950), Ong (U.S. Patent 5,426,378), Kelem et al. (U.S. Patent 6,170,821), Nishihara et al. '854 (U.S. Patent 6,842,854), Pleis et al. (U.S. Patent 7,287,112), Nishihara et al. '836 (U.S. Patent Application Publication 2005/0027836), Mita et al. (U.S. Patent Application Publication 2005/0108290), Hiramatsu et al. (U.S. Patent Application Publication 2007/0038971), Fujisawa et al. (U.S. Patent Application Publication 2007/0083733), and Sato (U.S. Patent Application Publication 2008/0122482).

Popli et al. show a configurable logic array that loads a user's configuration from a configuration file stored on an external memory device.

Ong shows a programmable logic device with a configuration memory that stores two or more sets of configuration data which are selectable by a switching circuit.

Kelem et al. show a programmable logic device capable of context switching of multiple configuration.

Nishihara et al. '854 corresponds to JP2001-202236 cited on ISR for PCT/JP05/03226.

Pleis et al. show a microcontroller with dynamically reconfigurable interrupts.

Nishihara et al. '836 corresponds to JP2003-029969 cited on ISR for PCT/JP05/03226.

Mita et al. corresponds to JP2003-198362 cited on ISR for PCT/JP05/03226.

Hiramatsu et al. reference is the corresponding U.S. Patent publication for a

foreign reference citing JP2001-202236.

Fujisawa et al. reference is the corresponding U.S. Patent publication for a foreign reference citing JP2001-202236.

Sato reference is the corresponding U.S. Patent publication for a foreign reference citing JP2001-202236.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

/ANH PHUNG/
Primary Examiner, Art Unit 2824